

SUBSTITUTE SPECIFICATION

LIQUID CRYSTAL DISPLAY DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a liquid crystal display device, and, more particularly, to a liquid crystal display device having an enlarged image display area.

5 Liquid crystal display devices are used in television sets, personal computers, and as displays for mobile terminals. An active matrix type of liquid crystal display device has transparent substrates disposed in opposition to each other with a liquid crystal interposed therebetween.

10 Fig. 20 is a diagram of the interconnection lines provided on and at the periphery of a transparent substrate of a typical liquid crystal display device of the type which is currently being manufactured. A liquid-crystal-side surface of one of the transparent substrates is provided with gate lines GW, which are disposed to extend in the x (lateral) direction and to be juxtaposed in the y (longitudinal) direction, and drain (source) lines DW, which are disposed to
15 extend in the y direction and to be juxtaposed in the x direction.

 The gate lines GW and the drain lines DW cross one another at right angles, and a switching element and a pixel electrode are formed in each area surrounded by adjacent ones of the gate lines GW and adjacent ones of the drain lines DW, thereby forming a so-called pixel. The switching element is turned on
20 by a scanning signal supplied from the corresponding one of the gate lines GW, and the pixel electrode is supplied with a video signal from the corresponding

one of the drain lines DW via the switching element. The areas that are defined by the gate lines GW and the drain lines DW constitute a pixel area AR.

Mobile terminals are being reduced more and more in size, whereas their image display areas are being enlarged more and more to realize better visibility of displayed information. For this reason, in a liquid crystal display device such as shown in Fig. 1, the proportion of the pixel area AR in the transparent substrate is increasing more and more, whereas the peripheral area surrounding the pixel area AR is decreasing more and more. In the typical liquid crystal display device, circuit chips for driving the liquid crystal (hereinafter referred to as drivers) and connecting lines are disposed in the peripheral area.

The gate lines GW and the drain lines DW are electrically connected to a gate driver and a drain driver via gate connecting lines GC and drain connecting lines DC, respectively. In a liquid crystal display device, if the display area is made larger, the distance between each of the gate connecting lines GC or the drain connecting lines DC becomes shorter because of the narrowing of the peripheral area, resulting in the problem of electrical shorting of the gate connecting lines GC or the drain connecting lines DC. In addition, if each of the gate connecting lines GC or the drain connecting lines DC is made thin, the problem of disconnection occurs.

Furthermore, as the peripheral area becomes narrower, an area in which the drivers are disposed becomes smaller. A gate driver GDr has gate signal output terminals on a long side closer to the pixel area AR. The gate connecting lines GC pass through a portion under the gate driver GDr and are connected to a gate common line GCOM. Accordingly, terminals for transmitting or receiving signals cannot be disposed on the side of the gate driver GDr that is closer to a short side of the panel PNL.

SUMMARY OF THE INVENTION

A liquid crystal display device according to the invention includes transparent substrates that are disposed in opposition to each other, with a liquid crystal interposed therebetween. One of the transparent substrates is provided with a plurality of gate lines that are disposed to extend in the x (lateral) direction and to be juxtaposed in the y (longitudinal) direction, and a plurality of drain (source) lines that are disposed to extend in the y direction and to be juxtaposed in the x direction. This substrate has a peripheral area which surrounds a pixel area formed by the plurality of gate lines and the plurality of drain lines.

10 The plurality of gate lines are connected to a plurality of gate connecting lines formed in the peripheral area. The plurality of gate connecting lines are stacked in the peripheral area. The gate connecting lines extend to a gate common line on a side different from a side where a driver is disposed. Drain connecting lines are disposed under a gate driver.

15 According to this construction, it is possible to provide a liquid crystal display device having a reduced peripheral area.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram of a substrate of a liquid crystal display device according to the invention;

Fig. 2 is a diagram of the layout of drain connecting lines according to the invention;

Fig. 3 is a cross-sectional view of the display device, taken along line I-I of Fig. 1;

25 Fig. 4 is a cross-sectional view of the display device, taken along line II-II of Fig. 1;

Fig. 5 is a cross-sectional view of the display device, showing another example of the construction of the gate connecting lines according to the invention;

Fig. 6 is a schematic diagram of a substrate of a liquid crystal display device having another structure according to the invention;

Fig. 7 is a cross-sectional view of the display device, taken along line III-III of Fig. 6;

Fig. 8 is a schematic diagram of a liquid crystal display device unit, which drives two liquid crystal display devices by means of one driver, according to the invention;

Fig. 9 is a cross-sectional view of a substrate of a liquid crystal display device according to the invention, taken along line IV-IV of Fig. 8;

Fig. 10 is a schematic diagram of a substrate of a liquid crystal display device according to a second embodiment of the invention;

Fig. 11 is a cross-sectional view of the display device, taken along line V-V of Fig. 10;

Fig. 12 is a cross-sectional view of the display device, taken along line VI-VI of Fig. 10;

Fig. 13 is a schematic diagram showing interconnection lines provided on and at the periphery of the substrate of the liquid crystal display device according to the invention;

Fig. 14 is a schematic diagram showing interconnection lines provided on and at the periphery of the substrate of the liquid crystal display device according to the invention;

Fig. 15 is a schematic diagram of a substrate of a liquid crystal display device having another construction according to the invention;

Fig. 16 is a schematic enlarged diagram of the liquid crystal display device of the invention in which a driver is disposed;

Fig. 17 is a schematic enlarged diagram of the liquid crystal display device of the invention, in which the driver DR is disposed;

5 Fig. 18 is a top plan view of the gate driver shown in Fig. 17;

Fig. 19 is a plan view showing the layout of the drain connecting lines DC; and

Fig. 20 is a diagram of interconnection lines provided on and at the periphery of a transparent substrate of a typical liquid crystal display device of
10 the type which is currently being manufactured.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A first embodiment of the invention will be described below with reference to the accompanying drawings.

15 In each of the embodiments, parts and portions having the same functions are denoted by the same reference numerals.

Fig. 1 is a schematic diagram of a substrate of a liquid crystal display device for a mobile terminal, according to the invention. The liquid crystal display device has an effective screen with a diagonal size of about 5.08 cm, and Fig. 1
20 shows a transparent substrate on which pixel electrodes are formed. The liquid crystal display device shown in Fig. 1 is an active matrix type of device.

The active matrix type of liquid crystal display device is provided with polygonal first and second substrates disposed in opposition to each other, with a liquid crystal layer being disposed between the first substrate and the second
25 substrate. Common electrodes are formed on the second substrate. Each of the

common electrodes and a corresponding one of the pixel electrodes form a capacitor to hold a voltage.

A liquid-crystal-side surface of the first substrate PNL1 is provided with gate lines GW that are disposed to extend in the x (lateral) direction and to be juxtaposed in the y (longitudinal) direction, and drain lines (or source lines) DW that are insulated from the gate lines GW and are disposed to extend in the y direction and to be juxtaposed in the x direction.

In each area which is surrounded by mutually adjacent ones of the gate lines GW and mutually adjacent ones of the drain lines DW, a switching element and a pixel electrode are formed to constitute a so-called pixel. The switching element is turned on by a scanning signal supplied from the corresponding one of the gate lines GW, while the pixel electrode is supplied with a video signal from the corresponding one of the drain lines DW via the switching element. One example of the switching element is a thin film transistor.

A gate driver GDr and a drain driver DDr are mounted on a panel PNL along one short side thereof by a flip chip attachment scheme. The gate driver GDr is connected to the gate lines GW, while the drain driver DDr is connected to the drain lines DW.

Fig. 1 shows part of the plurality of gate lines GW. In Fig. 1, there are a gate line GW1 for controlling the most distant pixels from the gate driver GDr, a gate line GW2 adjacent to the gate line GW1, a gate line GW4 for controlling the central pixels of the screen of the panel PNL, a gate line GW3 adjacent to the gate line GW4 and positioned on a more distant side from gate driver GDr, a gate line GW5 adjacent to the gate line GW4 and positioned on a side closer to the gate driver GDr, a gate line GW6 adjacent to the gate line GW5, a gate line GWm for controlling the closest pixels to the gate driver GDr, and a gate line GWm-1

adjacent to the gate line GWm. The gate lines GW1, GW2, GW3, GW4, GW5, GW6, GWm-1 and GWm are respectively electrically connected to gate connecting lines GC1, GC2, GC3, GC4, GC5, GC6, GCm-1 and GCm. The gate connecting lines GC1, GC2, GC3, GC4, GC5, GC6, GCm-1 and GCm are
5 connected to the gate driver GDr.

Fig. 1 shows part of the plurality of drain lines DW. In Fig. 1, there are drain lines DW1 and DWn, which are respectively disposed on lateral opposite ends of a pixel area AR. The area surrounded by the gate line GW1 and GWm and the drain lines DW1 and DWn is the pixel area AR. No pixels are formed in a
10 peripheral area AP of the panel PNL.

The panel PNL shown in Fig. 1 is a rectangular substrate having short sides and long sides. In the peripheral area AP thereof, the gate connecting lines GC and a common line VCL are disposed in an area GA1 along one of the long sides (hereinafter referred to as the first long side area GA1).
15 Charge-holding lines SW and a common line VCL are disposed in an area GA2 along the other of the long sides (hereinafter referred to as the second long side area GA2) in the peripheral area AP. The common lines VCL are electrically connected to the common electrodes that are disposed in opposition to the first substrate PNL1 via a common line connecting terminal VCP.

20 In the peripheral area AP, IC chips for driving the liquid crystal display device are fixed in an area DA1 along one of the short sides (hereinafter referred to as the first short side area DA1).

The driver circuit chip DDr, which is electrically connected to the drain lines DW (hereinafter referred to the drain driver) DDr) is disposed in an area
25 containing the central portion of the first short side area DA1. The drain lines DW and the drain driver DDr are interconnected by drain connecting lines DC.

Fig. 2 is a diagram showing the layout of the drain connecting lines DC in the peripheral area AP on the side where the drain driver DD_r is disposed. A first drain connecting line DC1 positioned on the leftmost side and a second drain connecting line DC2 adjacent to the first drain connecting line DC1 are spaced apart from each other by a distance DP. Since the first drain connecting line DC1 and the second drain connecting line DC2 are disposed in parallel with each other, the distance DP can be made constant, and the width of each of the drain connecting lines DC can be made constant. Accordingly, electrical short-circuiting and disconnection can be restrained from occurring in any of the drain connecting lines DC over the entire length thereof.

The interconnection resistances of the respective drain connecting lines DC are made uniform from a drain connecting line extending to the most distant position from the drain driver DD_r to a drain connecting line extending to the closest position. Since the interconnection resistances are uniform, the rounding of signal waveforms supplied from the drain driver DD_r to individual pixels is made uniform. Since the interconnection resistances are uniform, variations in display characteristic among the pixels can be reduced.

As the difference in length between each of the drain connecting lines DC is made smaller and the distance DP is made larger, the interconnection resistances of the respective drain connecting lines DC can be made uniform more easily. The distance DP can be calculated by $DP = \sin \theta_1 \times P$, where P is the pixel pitch. The pixel pitch P is a value to be determined according to the type of product, and the distance DP can be increased by increasing the angle θ_1 . Since the drain driver DD_r is disposed in the central portion of the first short side area DA1, the distance DP can be maximized.

The driver circuit chip (hereinafter referred to the gate driver) GDr, which is electrically connected to the gate lines GW, is disposed on the left side of the drain driver DDr with a space interposed therebetween. According to this construction, the drain driver DDr needs only to be mounted on one side of the first substrate PNL1, and the peripheral area AP of the first substrate PNL1 can
5 be made small on the other side on which no drivers are disposed.

The gate driver GDr has a rectangular shape with long sides parallel to the short sides of the panel PNL and short sides parallel to the long sides of the panel PNL. The gate connecting lines GC are connected to terminals provided
10 on the long and short sides of the gate driver GDr that are exposed to the display area AR.

Since part of the terminals are provided on the short side of the gate driver GDr, the long sides of the gate driver GDr can be made short, whereby an increase in the peripheral area AP can be restrained. In addition, since the long
15 sides of the gate driver GDr can be made short, the incident angle θ_1 of the drain connecting lines DC, with respect to the Y axis, can be increased, whereby the yield factor of manufacture can be improved.

The gate connecting lines GC1, GC2, GC3 and GC4 are connected to the upper half (more distant from the gate driver GDr) of the gate connecting
20 lines GC of the pixel area AR, while the gate connecting lines GC5, GC6, GCm-1 and GCm are connected to the lower half (closer to the gate driver GDr) of the gate connecting lines GC of the pixel area AR, and each of the gate connecting lines GC1, GC2, GC3 and GC4 is disposed to overlap a respective one of the gate connecting lines GC5, GC6, GCm-1 and GCm. In a first long side area
25 GA1, the gate connecting line GC1 and the gate connecting line GC5 overlap each other, the gate connecting line GC2 and the gate connecting line GC6

overlap each other, the gate connecting line GC3 and the gate connecting line GCm-1 overlap each other, and the gate connecting line GC4 and the gate connecting line GCm overlap each other.

In the first short side area DA1, the gate connecting line GC5 is insulated
5 from and crosses the gate connecting lines GC1, GC2, GC3 and GC4, which are connected to the upper half of the gate connecting lines GC.

Fig. 3 is a cross-sectional view taken along line I-I of Fig. 1.

The gate connecting lines GC1, GC2, GC3 and GC4 are connected to
the upper half (more distant from the gate driver GDr) of the gate connecting
10 lines GC of the pixel area AR and are respectively disposed to overlie the gate connecting lines GC5, GC6, GCm-1 and GCm, which are connected to the lower half (closer to the gate driver GDr) of the gate connecting lines GC of the pixel area AR.

As shown in Fig. 3, the underlying gate connecting lines GC5, GC6,
15 GCm-1 and GCm are formed on the panel PNL, and the overlying gate connecting lines GC1, GC2, GC3 and GC4 are respectively formed to overlie the underlying gate connecting lines GC5, GC6, GCm-1 and GCm. The gate connecting lines GC3 and GC4 are overlying gate lines which extend so as to climb over the underlying gate connecting lines GCm-1 and GCm, respectively.

20 The overlying gate connecting lines GC1, GC2, GC3 and GC4 and the underlying gate connecting lines GC5, GC6, GCm-1 and GCm are controlled in different manners.

Each of the underlying gate connecting lines GC5, GC6, GCm-1 and GCm has an oxide film 1 formed by oxidizing its surface. A first protective film 2,
25 for the purpose of providing an electrical insulation between the underlying gate connecting lines GC5, GC6, GCm-1 and GCm and the overlying gate connecting

lines GC1, GC2, GC3 and GC4, is formed on the oxide film 1. A second protective film 4 is formed on the overlying gate connecting lines GC1, GC2, GC3 and GC4. The protection of the gate connecting lines GC and the insulation thereof from other interconnection lines can be realized by the second protective film 4.

The pixel area AR of the panel PNL has the first gate line GW1 and the second gate line GW2, and the first gate connecting line GC1, which electrically connects the gate line GW1 to the liquid crystal driving circuit GDr, and the second gate connecting line GC2, which electrically connects the gate line GW2 to the liquid crystal driving circuit GDr, are disposed in the peripheral area AP. The first gate connecting line GC1 and the second gate connecting line GC2 are stacked in the thickness direction of the panel PNL, whereby the pixel area AR can be made narrow and the pixel area AR can be made large.

In addition, the width of each of the gate connecting lines GC can be made thick, whereby the disconnection of any of the gate connecting lines GC can be restrained. Furthermore, the distance between each of the gate lines GW can be made long, whereby the short-circuiting between the gate lines GW can be restrained.

Fig. 4 is a cross-sectional view taken along line I-I of Fig. 1.

The gate connecting line GC3 is formed on an amorphous silicon layer 3 that is formed on the first protective film 2. The gate connecting line GC3 overlaps part of the gate line GW3 and is electrically connected to the gate line GW3. The gate line GW3 has an oxide film 1 on its surface, but does not have an oxide film in the portion of the gate line GW3 that is connected to the gate connecting line GC3. In this construction, the gate line GW3 and the gate connecting line GC3 are electrically connected to each other.

Fig. 5 is a cross-sectional view showing another example of the construction of the gate connecting lines GC, taken along line I-I of Fig. 1. In Fig. 5, the overlying gate connecting lines GC1 to GC4 and the underlying gate connecting lines GC5 to GCm are disposed so as to be shifted from one another.

5 As shown in Fig. 5, each of the overlying gate connecting lines GC1 to GC4 is formed above the interspace between a respective pair of the underlying gate connecting lines GC5 to GCm, whereby it is possible to reduce the added capacitance which is applied between each of the overlying gate connecting lines GC1 to GC4 and a respective one of the underlying gate connecting lines
10 GC5 to GCm. Accordingly, it is possible to reduce the influence of waveform rounding and noise on the image quality.

Fig. 6 is a schematic diagram of the substrate of a liquid crystal display device having another structure according to the invention.

The gate connecting lines GC shown in Fig. 6 are arranged so that two
15 adjacent gate connecting lines, which are connected to each pair of gate lines that are adjacent to each other, are disposed in a vertically stacked manner. According to this structure, it is possible to reduce the number of crossings of the gate connecting lines GC near the gate driver GDr.

Fig. 7 is a cross-sectional view taken along line III-III of Fig. 6. The gate
20 connecting line GC1 adjacent to the gate connecting line GC2 is disposed over the gate connecting line GC2. The underlying gate connecting line GC2 has an oxide film 1 on its surface, and the top surface of the oxide film 1 is covered with the first protective film 2. The amorphous silicon layer 3 is formed on the first protective film 2. The underlying gate connecting lines GC and the overlying
25 gate connecting lines GC are positively insulated from each other by the first protective film 2 and the amorphous silicon layer 3.

Fig. 8 is a schematic diagram of substrates of a liquid crystal display device unit in which two separate liquid crystal display devices are driven by one drain driver.

The liquid crystal display device unit has a construction in which one
5 gate driver and one drain driver drive two liquid crystal display devices, i.e., the first liquid crystal display device and the second liquid crystal display device. The first liquid crystal display device and the second liquid crystal display device have a first pixel area AR1 and a second pixel area AR2, respectively.

The first liquid crystal display device has a liquid crystal layer between a
10 first substrate PNL1 and a second substrate PNL2, and the second liquid crystal display device has a liquid crystal layer between a third substrate PNL3 and a fourth substrate PNL4. Elements, such as gate lines, drain lines, gate connecting lines, drain connecting lines, switching elements and pixel electrodes, are formed on the first substrate PNL1 and the third substrate PNL3
15 of the substrates PNL1 to PNL4.

The gate driver GDr and the drain driver DDr are disposed in the first short side area DA1 of the first substrate PNL1. Flexible-printed-circuit-board connecting pads FPAD for connection to a flexible printed circuit board FPC are formed in an area DA2 of the peripheral area of the first substrate PNL1 on the
20 other short side thereof (hereinafter referred to as the second short side area DA2).

One end of the flexible printed circuit board FPC is connected to the flexible-printed-circuit-board connecting pads FPAD of the first substrate PNL1, while the other end of the flexible printed circuit board FPC is connected to the
25 flexible-printed-circuit-board connecting pads FPAD of the third substrate PNL3.

Gate connecting lines GMC and the drain connecting lines DC are connected to the flexible-printed-circuit-board connecting pads FPAD of the first substrate PNL1. The gate connecting lines GMC and the drain connecting lines DC are respectively connected to the gate lines and the drain lines of the third substrate PNL3 via the flexible printed circuit board FPC.

The gate connecting lines GMC for the second liquid crystal display device are connected to the gate driver GDr by an arbitrary number of lines (k lines). The gate connecting lines GMC for the second liquid crystal display device are disposed to overlie the gate connecting lines GC so that an arbitrary number of the gate connecting lines GMC are juxtaposed in ascending order from the first gate connecting line GC1, that is connected to the most distant gate line GW1 from the gate driver GDr. According to this construction, the number of crossings of the gate connecting lines GMC for the second liquid crystal display device and the gate lines GW is decreased, whereby the disconnection of the gate lines GW can be prevented.

The gate connecting lines GMC1 and GMCK for the second liquid crystal display device are respectively connected to gate lines GMW1 and GMk of the third substrate PNL3 via the flexible printed circuit board FPC.

Fig. 9 is a cross-sectional view of the first substrate PNL1, taken along line IV-IV of Fig. 8.

The gate connecting line GMC1, which is connected to the gate line GMW1 formed on the third substrate PNL3, is disposed to overlie the first gate connecting line GC1, which is connected to the gate line GW1 formed on the first substrate PNL1. The gate connecting line GMCK, which is connected to the gate line GMWk formed on the third substrate PNL3, is disposed to overlie the first

gate connecting line GCK, which is connected to the gate line GW_k formed on the first substrate PNL1.

Each of the gate connecting lines GC has an oxide film 1 on its surface, and the oxide film 1 is covered with the first protective film 2. The amorphous silicon layer 3 is formed on the first protective film 2. The underlying gate connecting lines GC and the overlying gate connecting lines GMC are positively insulated from each other by the first protective film 2 and the amorphous silicon layer 3.

A second embodiment of the invention will be described below.

Fig. 10 is a diagram of a glass plate GL including a substrate of a liquid crystal display device according to the second embodiment of the invention. The panel PNL is cut from the glass plate GL on which thin film transistors and peripheral interconnection lines are formed. The gate lines GW are connected to a gate common line GCOM that is disposed outside of the panel PNL. A voltage is supplied from the gate common line GCOM to form the oxide film 1 on the surface of each of the gate lines GW (anodic oxidation).

In order to enable static electricity to escape during the manufacturing process, the drain lines DW extend to the second short side area DA2 opposed to the first short side area DA1 in which the drain driver DDr is disposed, and they are electrically connected to a drain common line DCOM beyond a short side of the panel PNL.

The charge-holding lines SW are electrically connected to the gate common line GCOM, which is disposed outside of the panel PNL. The charge-holding lines SW extend to the gate common line GCOM from the same side as the gate lines GW. A voltage is supplied from the gate common line GCOM to oxidize the surface of each of the gate lines GW. The gate lines GW

and the charge-holding lines SW are disposed in parallel to one another, and the common line VCL is disposed to cross the gate lines GW and the charge-holding lines SW at right angles.

Fig. 11 is a cross-sectional view taken along line V-V of Fig. 10. The gate lines GW4 and GW5 and charge-holding lines SW4 and SW5 are formed on the panel PNL. The gate lines GW4 and GW5 and the charge-holding lines SW4 and SW5 are formed of aluminum. The surface layer of aluminum is oxidized. In addition, the protective film 4 is formed to cover the gate lines GW4 and GW5 and the charge-holding lines SW4 and SW5. The protective film 4 is formed to protect the lines GW4, GW5, SW4 and SW5 and to insulate the lines GW4, GW5, SW4 and SW5 from one another.

Fig. 12 is a cross-sectional view taken along line VI-VI of Fig. 10. The gate lines GW (GW4 and GW5) and the charge-holding lines SW (SW4 and SW5) are formed on the substrate PNL. The gate lines GW4 and GW5 and the charge-holding lines SW4 and SW5 are formed of aluminum.

Each of the gate lines GW (GW4 and GW5) has an oxidized surface layer. The first protective film 2 is stacked on the gate lines GW (GW4 and GW5), each having the oxidized surface layer. The amorphous silicon layer 3 is stacked on the first protective film 2.

The charge-holding lines SW (SW4 and SW5) are formed at the same level as the gate lines GW (GW4 and GW5), and an oxide layer does not overlie the portion of any of the charge-holding lines SW (SW4 and SW5) that is connected to the common line VCL. During anodic oxidation, the portion of each of the charge-holding lines SW (SW4 and SW5) that is connected to the common line VCL is covered with a resist so that the oxidation of the connection portion is prevented.

Holes are formed in the first protective film 2 and the amorphous silicon layer 3 formed on the charge-holding lines SW (SW4 and SW5).

The common line VCL is formed on the amorphous silicon layer 3. Since the first protective film 2 and the amorphous silicon layer 3 overlie the gate lines GW (GW4 and GW5), the gate lines GW (GW4 and GW5) are insulated from the common line VCL. The holes are formed in the first protective film 2 and the amorphous silicon layer 3 that is formed on the charge-holding lines SW (SW4 and SW5), thereby providing electrical connection between the common line VCL and the charge-holding lines SW (SW4 and SW5).

The second protective film 4 is formed on the common line VCL in order to protect the common line VCL and insulate the common line VCL from other lines.

In the structure shown in Fig. 12, the gate lines GW (GW4 and GW5) and the charge-holding lines SW (SW4 and SW5) are electrically connected to the gate common line GCOM for anodic oxidation, whereby an oxide layer can be formed on each of the gate lines GW (GW4 and GW5) and the charge-holding lines SW (SW4 and SW5), and the charge-holding lines SW (SW4 and SW5) can be connected to the common line VCL.

When the glass plate GL is cut along the external shape of the panel PNL, the gate lines GW are divided into individual gate lines.

Since the gate lines GW and the charge-holding lines SW that are connected to the gate common line GCOM for anodic oxidation are disposed on the same side as the common line VCL, lines which have heretofore been disposed under the gate driver GDr and connected to the gate common line GCOM in the related art become unnecessary.

Fig. 13 is a diagram of interconnection lines provided on and at the periphery of the panel PNL of the liquid crystal display device. A cross-section of the structure within the circled area T in Fig. 13 is shown in Fig. 12.

The common line VCL extends in parallel with the gate lines GW.

5 In the liquid crystal display device shown in Fig. 13, the gate lines GW and the charge-holding lines SW are connected to the gate common line GCOM in the second short side area DA2, opposite to the first short side area DA1 in which the gate driver GDr is disposed.

10 In addition, in the liquid crystal display device shown in Fig. 13, since the drain lines DW, that are connected to the drain common line DCOM and the gate lines GW, and the charge-holding lines SW, that are connected to the gate common line GCOM, are disposed on only one side, troubles due to static electricity can be reduced. Specifically, it is possible to reduce troubles, such as the generation of static electricity, which tends to cause variations in the
15 thresholds of individual TFTs and cause non-uniformity in the display. In addition, it is possible to reduce disconnection due to electrolytic corrosion.

The gate lines GW and the charge-holding lines SW, connected to the gate common line GCOM, are disposed to extend toward the gate common line GCOM on a side except the side where the gate driver GDr is mounted.

20 According to the second embodiment, since the gate lines GW and the charge-holding lines SW, which are connected to the gate common line GCOM, are disposed on the side except the side where the gate driver GDr is mounted, lines which have heretofore been disposed under the gate driver GDr and connected to the gate common line GCOM become unnecessary. Accordingly,
25 the gate driver GDr can have terminals disposed on all sides, and it can be reduced in size.

Each of the charge-holding lines SW has an oxide film in the display area AR. This is because, since the charge-holding lines SW cross the drain lines DW at right angles, similar to the gate lines GW crossing the drain lines DW at right angles, the charge-holding lines SW need to have the same structure as the gate lines GW. Short-circuiting of the charge-holding lines SW can be restrained by the oxide film formed as an insulating layer.

The common line VCL is provided to feed a common voltage to the common electrodes and to apply a constant voltage to the charge-holding lines SW. If the resistance of the common line VCL with respect to the charge-holding lines SW greatly differs between the top and the bottom of the screen of the panel PNL, a voltage drop will occur, resulting in luminance irregularity. Accordingly, the common line VCL is made thick to reduce the difference in the resistance of the common line VCL with respect to the charge-holding lines SW between the top and the bottom of the screen.

Fig. 14 is a diagram showing the interconnection lines provided on and at the periphery of the panel PNL of the liquid crystal display device. A cross-section of the structure within each of the circled areas T and U in Fig. 14 is shown in Fig. 12.

The gate lines GW and the charge-holding lines SW which are connected to the gate common line GCOM are disposed to extend to the gate common line GCOM in the first short side area DA1, where the gate driver GDr is mounted, and in the second short side area DA2. In the liquid crystal display device shown in Fig. 14, half of the lines GW and SW connected to the gate common line GCOM, which half is closer to the gate driver GDr, extend to the gate common line GCOM in the first short side area DA1 where the gate driver GDr is mounted. On the other hand, the half of the lines GW and SW that are

connected to the gate common line GCOM, which half is more distant from the gate driver GDr, extend to the gate common line GCOM in the second short side area DA2. According to the structure shown in Fig. 14, the second long side area GA2 can be made narrow.

5 Fig. 15 is a diagram showing the layout of interconnection lines in the case where the gate driver GDr and the drain driver DDr are formed on one chip. Fig. 15 shows interconnection lines inside the panel PNL, as well as interconnection lines outside the panel PNL which are being manufactured.

10 The gate connecting lines GC are connected to the right and left sides of a driver Dr. The half of the gate lines GW that are more distant from the driver Dr extend in parallel with the gate lines GW and are connected to the gate common line GCOM, i.e., they pass through the first long side area GA1 and are connected to the gate common line GCOM. The gate connecting lines GC that are connected to the half of the gate lines GW that are closer to the driver Dr
15 extend into a portion under the driver Dr and are connected to the gate common line GCOM.

 According to the structure shown in Fig. 15, the number of interconnection lines passing through the portion under the driver Dr can be reduced.

20 A third embodiment of the invention will be described below.

 Fig. 16 is a schematic enlarged view of part of the interconnection lines of the panel PNL in which the driver Dr is disposed. The gate driver GDr and the drain driver DDr are mounted on the panel PNL by a flip chip attachment scheme.

25 Drain connecting lines DC1a and DC2a are respectively connected to terminals that are disposed on the short side of the drain driver DDr that is closer

to the gate driver GDr. The drain connecting line DC1a is connected to the terminal that is disposed at the closest position to the short side of the panel PNL, while the drain connecting line DC2a is connected to the terminal disposed at the closest position to the pixel area AR. These drain connecting lines DC1a and DC2a are disposed so as to avoid the gate driver GDr.

The drain connecting line DC1a is at an angle $\theta 2$ with respect to the pixel area AR in the vicinity of the pixel area AR. Namely, the drain connecting line DC1a is at the angle $\theta 2$ with respect to a line parallel to the gate lines GW in the vicinity of the pixel area AR. In addition, the drain connecting line DC1a is at an angle $\theta 3$ with a line parallel to the gate lines GW in the vicinity of the drain driver DDr.

The drain connecting line DC3a is connected to a terminal which is disposed at the closest position to the gate driver GDr, of all the terminals provided on a long side of the drain driver DDr. The drain connecting line DC3a is at an angle $\theta 4$ with respect to the line parallel to the gate lines GW. The relationship between the angle $\theta 2$ and the angle $\theta 3$ is $\theta 2 < \theta 3$. According to this construction, the peripheral area AP can be made narrow.

Fig. 17 is a schematic enlarged view of part of the interconnection lines of the panel PNL in which the driver Dr is disposed.

The drain connecting lines DC, which are respectively electrically connected to terminals disposed on the short side of the drain driver DDr that is closer to the gate driver GDr pass through a portion under the gate driver GDr, and are electrically connected to the drain lines DW.

Drain connecting lines DC1b and DC2b are respectively connected to the terminals disposed on the short side of the drain driver DDr that is closer to the gate driver GDr. The drain connecting line DC1b is connected to the terminal

that is disposed at the closest position to the short side of the panel PNL, while the drain connecting line DC2b is connected to the terminal that is disposed at the closest position to the pixel area AR.

In Fig. 17, the drain connecting line DC1b is at an angle $\theta 5$ with respect to a line parallel to the gate lines GW in the vicinity of the pixel area AR. The drain connecting lines DC1b and DC2b, which are connected to the short side of the drain driver DDr that is closer to the gate driver GDr, are disposed so as to be partly parallel to the gate lines GW. These drain connecting lines DC1b and DC2b pass through a portion under the gate driver GDr.

The drain connecting line DC3b is connected to a terminal which is disposed at the closest position to the gate driver GDr, of all the terminals provided on a long side of the drain driver DDr. The drain connecting line DC3b is at an angle $\theta 6$ with respect to the line parallel to the gate lines GW.

These drain connecting lines DC1b and DC2b pass through the portion under the gate driver GDr. Accordingly, the angle $\theta 5$ between each of the drain connecting lines DC1b and DC2b and the pixel area AR can be increased.

Therefore, the distance between each adjacent one of the drain connecting lines DC can be made large, whereby the short-circuiting between the drain lines DW can be reduced. The angle $\theta 5$ shown in Fig. 17 can be made larger than the angle $\theta 4$ shown in Fig. 16.

According to this construction, the peripheral area AP can be made narrow, and the short-circuiting between the drain lines DW can be restrained. In addition, the disconnection of the drain lines DW can be restrained.

The third embodiment may also be applied to a liquid crystal display device of the type in which the gate driver GDr and the drain driver DDr are

mounted on the panel PNL as two independent drivers according to the other embodiments.

Fig. 18 is a top plan view of the gate driver GDr in Fig. 17, showing the layout of terminals.

5 The gate driver GDr is rectangular, and terminals 8 are provided on each of the sides of the gate driver GDr. A first output terminal group GOUT1 is disposed on one of the short sides of the gate driver GDr, while a second area 6, through which the drain connecting lines DC can pass, and a gate signal terminal group G2 are disposed on the other short side. The short side where the second
10 area 6 and the gate signal terminal group G2 are disposed is the short side closer to the drain driver DDr.

A second output terminal group GOUT2 and a first area 5 through which the drain connecting lines DC can pass are disposed on one of the long sides of the gate driver GDr, particularly on the long side closer to the pixel area AR. A
15 third area 7, through which lines pass for anodic oxidation of the gate lines GW, and an input/output terminal group G1 of the gate driver GDr are disposed on the other long side of the gate driver GDr.

The terminals 8 provided in the first area 5 and the second area 6 are dummy terminals, and the drain lines DW may also be disposed under the first
20 area 5 and the second area 6, so that electrical interference between the internal circuit of the gate driver GDr and the drain lines DW can be prevented.

According to the above-described construction, it is possible to reduce the peripheral area AP surrounding the pixel area AR.

Fig. 19 is a plan view of the third embodiment, showing the layout of the
25 drain connecting lines DC.

Part of the drain connecting lines DC that are electrically connected to the short side of the drain driver DD_r that is closer to the gate driver GD_r pass through a portion under the gate driver GD_r and are electrically connected to the drain lines DW. Two of the drain connecting lines DC shown in Fig. 19, i.e., a
5 drain connecting line DC1c positioned on the outermost side and a drain connecting lines DC2c adjacent to the drain connecting line DC1c, pass through a portion between dummy terminals and are connected to the drain lines DW.

According to the above-described construction, it is possible to reduce the peripheral area AP of the panel PNL that surrounds the pixel area AR.